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D0 Muon Fanout Card Tester

Technical Specification
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1. Introduction

The Muon Fanout Card Tester (MFCT) is designed to provide a tool for automatic testing of the Muon Fanout Card (MFC). It is 9U x 280 mm card with **A24:D16** VME slave interface.

2. Mechanical specification

A front-panel of the MTFC is shown in the Figure 1. The MFCT has three coaxial

Figure 1 Front panel of the MFCT.

output connectors: one from SCL daughter card and two identical connectors from the HOTLink™ transmitter. There are two multi-pin connectors: a test socket and SCL daughter card status connector. A reset (RST) button generates equivalent of the power-on reset signal. There are eighteen LED indicators located on the front panel in the following order:

- **"VME**" - VME command decoded
- **"SEQ**" - sequencer is running
- **"HL"** - HOTLink transmitter is turned on
- **"L1A" -** L1 Accept generated by sequencer
- **"L2A" -** L2 Accept generated by sequencer
- **"L2R" -** L2 Reject generated by sequencer
- **"INIT" -** J2 INIT detected
- **"RF" -** J2 RF detected
- **"ENC" -** J2 encoded timing detected
- **"STR" -** J2 STR detected
- **"L1A" -** J2 L1 Accept detected
- **"L2A" -** J2 L2 Accept detected
- **"L2R" -** J2 L2 Reject detected
- **"FC" –** J2 First Crossing signal detected
- **"GAP" -** J2 GAP signal detected
- **"SGAP" -** J2 SGAP signal detected
- **"SPARE" –** not used yet
- **"+5V" -** +5V present on the backplane

2. Pattern memory data format

Pattern memory has a repeated pattern of five 16-bit words (see below), which define trigger decision data. Please note that MFC and TFC modules have similar trigger data patterns, but only consist of four 16-bit words. The end of the sequence is indicated by a terminator word.

- *Pointer crossing number* (relative address = 0)

15	***14***	***13***	***12***	***11***	***10***	***9***	***8***	***7***	***6***	***5***	***4***	***3***	***2***	***1***	***0***
0	0	0	0	0	0	0	0	X7	X6	X5	X4	X3	X2	X1	X0

X7..X0 - Pointer crossing number

- *Pointer turn number* (relative address = 2)

15	***14***	***13***	***12***	***11***	***10***	***9***	***8***	***7***	***6***	***5***	***4***	***3***	***2***	***1***	***0***
T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0

T15..T0 - Pointer turn number

- *Event crossing number* (relative address = 4)

15	*14*	*13*	*12*	*11*	*10*	*9*	*8*	*7*	*6*	*5*	*4*	*3*	*2*	*1*	*0*
1	L2R	L2A	L1A	0	0	L2Q	L1Q	X7	X6	X5	X4	X3	X2	X1	X0

L1Q - L1 Accept qualifier bit (1 – true)

L2Q - L2 Accept qualifier bit (1 – true)

XP7..XP0 - Event crossing number

L1A - L1 Accept bit (1 – true)

L2A - L2 Accept bit (1 – true)

L2R - L2 Reject bit (1 = true)

- *Event turn number* (relative address = 6)

15	*14*	*13*	*12*	*11*	*10*	*9*	*8*	*7*	*6*	*5*	*4*	*3*	*2*	*1*	*0*
T15	T14	T13	T12	T11	T10	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0

T15..T0 - Event turn number

- *Event transfer number* (relative address = 8)

15	*14*	*13*	*12*	*11*	*10*	*9*	*8*	*7*	*6*	*5*	*4*	*3*	*2*	*1*	*0*
Q15	Q14	Q13	Q12	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0

Q15..Q0 - Event transfer number (not used in the TFC mode)

- *Terminator word* (even relative address)

15	*14*	*13*	*12*	*11*	*10*	*9*	*8*	*7*	*6*	*5*	*4*	*3*	*2*	*1*	*0*
0	0	0	0	TM	0	0	0	0	0	0	0	0	0	0	0

TM - Terminator bit (1 – true)

3. MFC Tester registers

The MFC Tester requires initialization from the VME bus. The module has standard **A24:D16** VME slave interface. The following is a list of the internal registers accessible via VME commands (the relative hex address shown). By default, all registers support reads and writes unless specifically commented.

- *FIFO storage register*[*)], *FIFOR* ($0800)

15	*14*	*13*	*12*	*11*	*10*	*9*	*8*	*7*	*6*	*5*	*4*	*3*	*2*	*1*	*0*
NC	NC	NC	NC	TER	L2R	L2A	L1A	X7	X6	X5	X4	X3	X2	X1	X0

X0..X7 - Trigger decision crossing number

L1A - L1 Accept indicator (1 - true)

L2A - L2 Accept indicator (1 - true)

L2R - L2 Reject indicator (1 - true)

TER - Timing error bit (1 true)

*) Note: reads and writes to this address increment FIFO's address pointer

- *MFCT control register, CSR0* ($1000)

15	*14*	*13*	*12*	*11*	*10*	*9*	*8*	*7*	*6*	*5*	*4*	*3*	*2*	*1*	*0*
NC	NC	NC	NC	NC	NC	SST	SEN	FCL	CER	RSQ	BRS	NC	NC	NC	NC

BRS - Board reset (write 1)

RSQ - Sequencer reset (write 1)

CER - Clear error bits (write 1)

FCL - Clear FIFO storage pointer (write 1)

SEN - Enable sequencer (0 – disable, 1 – enable)

SST - Single step mode (write 1)

- *HOTLink transmitter control register CSR1* ($1002)

15	*14*	*13*	*12*	*11*	*10*	*9*	*8*	*7*	*6*	*5*	*4*	*3*	*2*	*1*	*0*
NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	NC	SVS	BSE	TEN

TEN - Transmitter enable (1 – enable)

BSE - BIST test enable (1 – enable)

SVS - Send violation symbol

- *J2 status/control register CSR2* ($1004)

15	*14*	*13*	*12*	*11*	*10*	*9*	*8*	*7*	*6*	*5*	*4*	*3*	*2*	*1*	*0*
ER2	ER1	BS2	BS1	NC	NC	SRQ	VBD	SLV	INIT	STE	SGE	GPE	FCE	RF	ENC

ENC - Encoded timing detected (read only)

RF - RF detected (read only)

FCE - First Crossing error (1 – error, read only)

GPE - Gap error (1 – error, read only)

SGE - Sync Gap error (1 – error, read only)

STE - STR error (1 – error, read only)

INIT - INIT level (1 – active, read only)

SLV - Slave Ready level (1 – active, read only)

VBD - VBD Done level (1 – active, 0 – inactive)

SRQ - SRQ level (1 – active, 0 – inactive)

BS1 - Busy 1 level (1 – active, 0 – inactive)

BS2 - Busy 2 level (1 – active, 0 – inactive)

ER1 - Error 1 level (1 – active, 0 – inactive)

ER2 - Error 2 level (1 – active, 0 – inactive)

- *FIFO storage memory address/status register CSR3* ($1006)

15	*14*	*13*	*12*	*11*	*10*	*9*	*8*	*7*	*6*	*5*	*4*	*3*	*2*	*1*	*0*
NC	NC	NC	NC	NC	NC	NC	OVF	A7	A6	A5	A4	A3	A2	A1	A0

A0..A7 - FIFO storage memory address

OVF - Overflow flag bit (1 – overflow)

4. Software requirements

The MFCT has power-up reset feature that sets initial value to the internal registers and resets the module. A VME SYSRESET or BRS bit in CSR0 produce the same effect. Initialization of the module can be done by writing 1 to bits RSQ, CER and FCL of CSR0. BRS should be used separately as an emergency measure.

The MFCT FIFO storage will be filled with Trigger Framework decisions detected at the J2 backplane. The depth of the FIFO memory is 256 words. The FIFO memory address is incremented automatically at each read or write. After 256th word is written to the memory, the address is rolled through zero and continues at the beginning of the memory. Each trigger decision occupies one data word in the memory.

A routine to read out contents of the FIFO storage should use the FIFO storage memory address register (CSR3) to determine how many words to read out. The value of the register has to be set to zero before readout can start, otherwise old stale data from the memory corresponding current address value will be read out. A FIFO memory test also will be useful for verifying the MFCT itself. Such a test could use a sequence of 256 writes to fill memory in and 256 reads to read it out.

Access to all MFCT registers will be useful at the beginning of the production tests. The expectation is that after initial testing the code for the MFCT will be a part of the COMMMFC code. After some experience of working with the MFCT is accumulated, we could specify an automatic testing procedure that can be implemented as a separate code or a part of the COMMMFC code.

Table 1. Muon Fanout Card Tester VME Address Map

Starting Address	Size (bytes)	Comment
Card Base Address + 000000	1K	Sequencer memory
Card Base Address + 000800	2	J2 data FIFO storage register
Card Base Address + 001000	2	MFCT control register
Card Base Address + 001002	2	HOTLink control register
Card Base Address + 001004	2	J2 status/control register